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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,288	06/10/2005	Joachim Christian Reiner	CH02 0037 US	9407

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

NOTIFICATION DATE	DELIVERY MODE
08/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,288	REINER, JOACHIM CHRISTIAN	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,9,10 and 16* is/are rejected.

7)☒ Claim(s) *2,4-8,11-15 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
AU 2827

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 31, 2007, claims 1-20 are active in this application as a result of the addition of claims 11-20.

Claim Objections

2. Claims 2, 4-8, 11-15 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections- 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 3, 9 and 16 are rejected under 35 U.S.C 102(b) as being anticipated by Okamoto [U.S. Patent # 5,781,489].

With respect to claim 1, Okamoto disclose, in figure 1, one-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor [2] and an MOS memory transistor [MCT] connected in series between a voltage supply line [electrode coupled to 11N1 from 2] and ground [source/drain electrode], and further comprising programming means [column selection signal] for applying voltages to a gate of said selection transistor, to a gate of said memory transistor [word line] and to said voltage supply line [via source/drain of 11N1], which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

With respect to claim 3, Okamoto disclose, in figure 1, that said MOS transistors are NMOS (N-channel metal-oxide semiconductor) transistors.

With respect to claim 9, Okamoto disclose, in figure 1, that the entire device is of MOS technology, and therefore, it is can be reasonably assumed that such a device is applicable to a CMOS device.

With respect to claim 16, Okamoto disclose, in figure 1, said programming means require a setup procedure for initiating their operation, which setup procedure comprises

more steps than applying one predetermined voltage level to said programming means. It is noted that the word and selection lines have potentials applying to the gates of the selection and memory transistors.

3. Claim 10 is rejected under 35 U.S.C 102(b) as being anticipated by Okamoto [U.S. Patent # 5,781,489].

With respect to claim 10, Okamoto disclose, in figure 1, a method for programming a one-time programmable memory, which memory comprises an MOS (metal-oxide semiconductor) selection transistor [2] and an MOS memory transistor [MCT] connected in series between a voltage supply line [electrode of 11N1 coupled to source/drain of 2] and ground [electrode coupled to source/drain of MCT], said method comprising applying voltages [via column selection signal] to a gate of said selection transistor, to a gate of said memory transistor [via wordline] and to said voltage supply line [via 11N1], which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. Further, it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

Allowable Subject Matter

4. The following is an Examiner's statement of reasons for the indication of allowable

subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Programming means comprise means for first applying a predetermined voltage to said gate of said memory transistor and for then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.
- At least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device. •Programming means require a setup procedure for initiating their operation, which setup procedure comprises more steps than applying one predetermined voltage level to said programming means.
- Programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.
- readout means for applying a high voltage to said gate of said selection transistor, for applying a low voltage to said gate of said memory transistor, for applying a readout voltage to said voltage supply line, for detecting a current through said transistors resulting with said applied voltages, for comparing said

detected current with a predetermined current value, and for providing an indication that said memory transistor is programmed in case it is determined that said detected current exceeds said predetermined current value.

- a plurality of memory cells, each of said memory cells including a respective selection transistor and a respective memory transistor connected in series between said voltage supply line and ground, wherein said programming means are suited to apply voltages to said memory cells forcing any selected one of said memory transistors into a snap-back mode resulting in a current thermally damaging a drain junction of the respective memory transistor.
- applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line comprises first applying a predetermined voltage to said gate of said memory transistor and then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.
- at least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage supply and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device.

- programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.

Conclusion

When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
August 13, 2007